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Solid Logic Technology: Versatile, High-Performance Microelectronics*

Abstract: A new microelectronics packaging technique, called Solid Logic Technology (SLT), utilizes silicon planar glass-encapsulated transistors and diodes, and graphic arts techniques for producing high-quality, passive components having tight tolerances. The result is a process permitting the low-cost realization of a variety of versatile, high-performance circuit modules.

The salient features of SLT are described: the unique form of the semiconductor devices, the module fabrication process, and some performance results. In addition, insight is provided to the range of components that may be fabricated with this technology, i.e., inductors, capacitors and high-power transistors. Examples are shown of specific high-speed, high-density and complex circuit packages.

Introduction

A new microelectronics technique called Solid Logic Technology, or SLT, is utilized in the new family of IBM/360 computers. This new technology provides a hybrid, integrated circuit module which combines discrete, glass-encapsulated silicon transistors and diodes with stencil-screened land patterns and precision passive components. The semiconductor devices are fabricated and tested separately, permitting precise parameter control. In the fabrication process these devices are attached to ceramic substrates containing tight-tolerance passive elements. The resultant module is a high-performance, minimum-power circuit in which parasitic interactions are minimized because of the electrical isolation of the discrete components. The design makes feasible hybrid, integrated circuits having close to maximum performance.

The configuration of the semiconductor chip device is the most novel aspect of the technology. The transistors and diodes designed for this approach incorporate a protective encapsulating layer of glass. Contacts from the active regions are brought out through openings in the glass layer to solderable terminations. The semiconductor

chips are attached to terminations in the substrate conductor pattern by a solder reflow process. These features permit low fabrication cost and a great flexibility of circuit configurations with minimum trade-off of circuit performance.

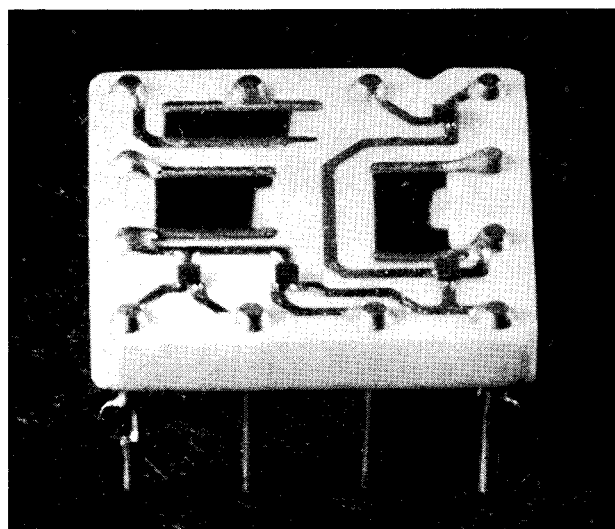
This paper discusses the major features of the technology. The ease and flexibility with which circuit modules are fabricated will be seen. Finally, it will be shown that there is an unusual versatility of applications because of the broad variety of passive devices and the ability to adapt package dimensions to match the application.

Transistor-diode-resistor module

The major features of an SLT module are best understood by reviewing in this section the procedure, step by step, that is used in the fabrication of a typical computer circuit module, an AND/OR INVERT (AOI) logic block. In the AOI circuit, an average logic delay of 20 nsec is characteristic when fan-in and fan-out ratios of 5 are provided. A completed AOI module is shown in Fig. 1a and the circuit diagram in Fig. 1b.

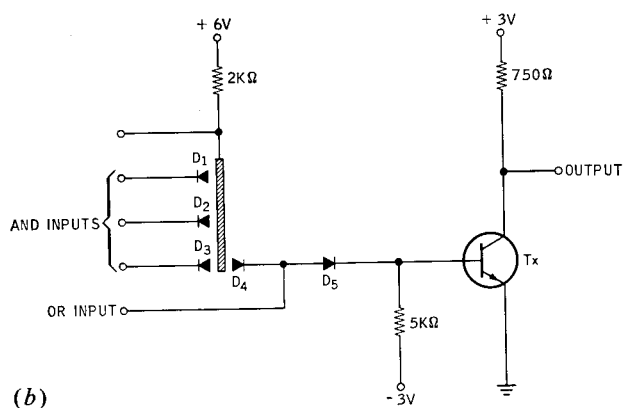
The unique configuration of the silicon devices used in the SLT circuits is illustrated in Fig. 2. The chip transistors

* Based in part on paper by Davis, Harding and Schwartz, "An Approach to Low Cost, High Performance Microelectronics," presented at Western Electronic Show and Convention, San Francisco, August 20, 1963.



(a)

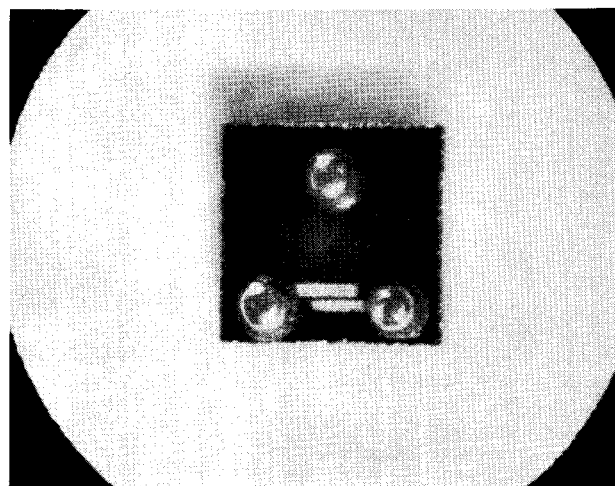
Figure 1 AND/OR INVERT logic module. (a) Completed AOI module, without overcoating. (b) Logic circuit.



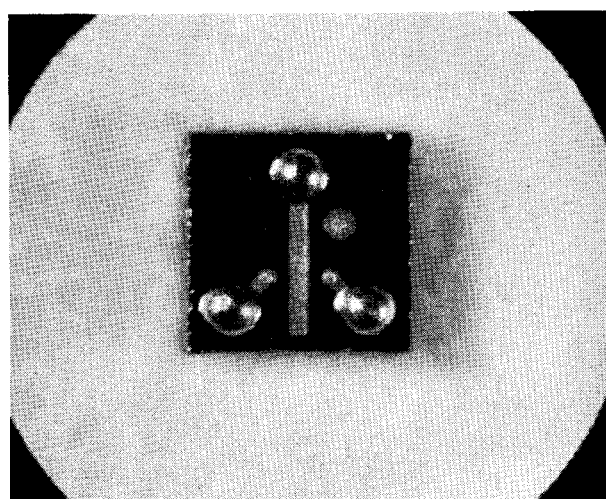
(b)

Power dissipation in mW

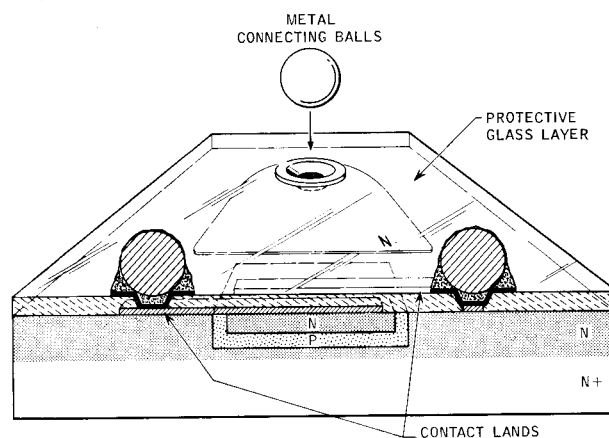
	On	Off	
Resistors	28	19	(All R: 5%)
Transistor	7	0	
D_1, D_2, D_3	0	2	
D_4	1	1	
D_5	$\frac{1}{2}$	$\frac{1}{2}$	
Total	37	23	



(a)



(b)



(c)

Figure 2 Glassed semiconductor chip devices. (a) Transistor. (b) Diode. (c) Cross section of transistor.

and diodes are silicon planar glass-encapsulated devices with all external terminals on one surface. Figure 2a is a view of the transistor and Fig. 2b of the diode, showing the side with the external terminals. Dual diodes in single-chip form are used because of their obvious space-saving advantages over single-chip diodes. Figure 2c shows a sketch, not to scale, of a cross section of the transistor.

• Transistor and diode fabrication

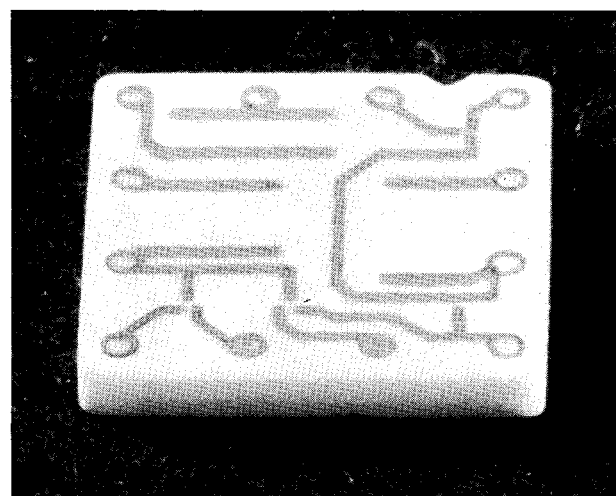
As is usually the case for devices of this type, hundreds of transistors or diodes are fabricated simultaneously on a single wafer of silicon. The semiconductor devices are produced using the conventional methods of masking, etching and diffusion. We depart from conventional techniques in fabricating the contacts and terminations. Note from Fig. 2c that contact lands extend away from the small-geometry emitter and base. These lands must be capable of withstanding high temperatures because in the next step the device undergoes a novel glassing¹ operation.

Contacts to the emitter base and collector regions are accomplished with solderable metal balls.² To attach these balls to the transistor, holes are etched through the glass layer to make available small regions of the emitter base and collector land contacts. A metallic layer is evaporated to cover the hole in the glass and extend out on the glass surface. The purpose of this layer is to contact the metal land in the hole and to anchor the metal ball in position by means of an intermediate layer of evaporated solder. We refer to this as the *ball-limiting layer*. Each wafer is placed beneath a jig so that balls may be placed into holes in the jig for alignment with the ball-limiting layer on the wafer. When heat is applied to the wafer, the solder film fuses, attaching each ball to the wafer. In the final step, each wafer is cut into individual chip devices. On each chip, the ball contacts to each active region are available on a single surface. These balls serve ultimately as a means for electrical contact and mechanical attachment when the chips are attached to the substrate.

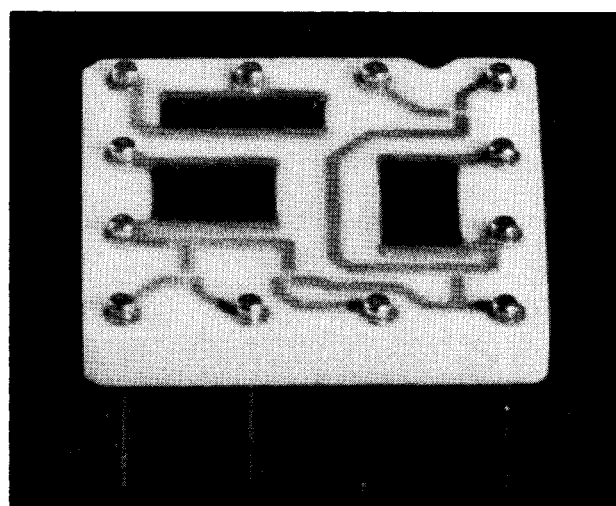
The transistors are completely tested before being committed to a module. They may be subjected to temperatures in excess of 300°C, during the process of fusing them to the circuit substrate, without appreciable change in their electrical or mechanical properties. Data on the stability of these devices under high humidity and other stress conditions are given in the section entitled "Some Test Results".

• Passive components

The processes employed to produce the AOI module passive components substrate begin with a ceramic substrate, nominally 0.455" × 0.455" × 0.060". This substrate contains 12 holes into which pins will later be in-



(a)

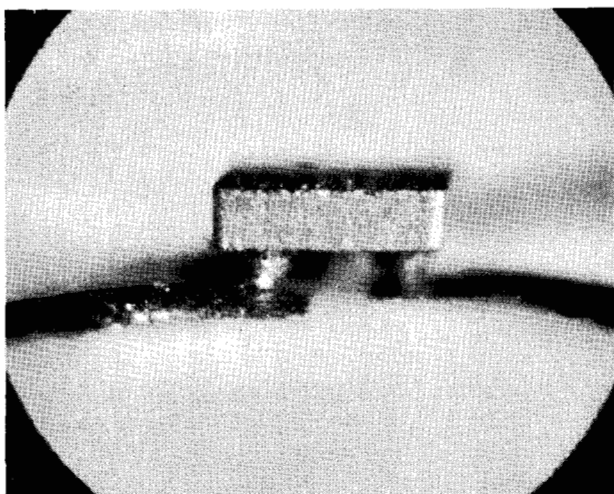


(b)

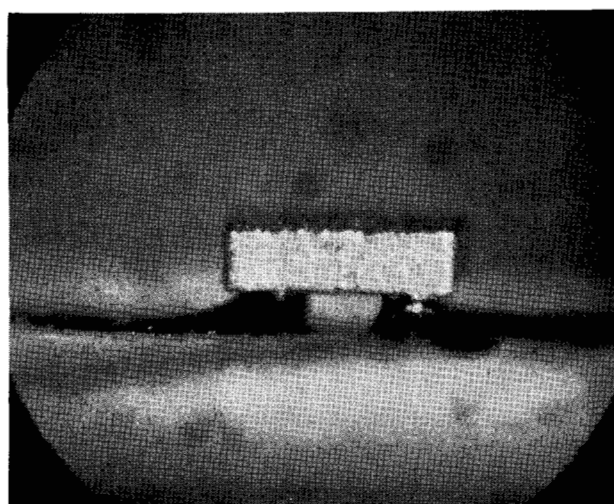
Figure 3 Substrate in various stages of processing. (a) With land pattern printed. (b) After pin insertion. (c) Side view of transistor chip on solder lands before soldering. (d) Transistor chip after soldering. (e) Complete module after overcoating.

serted. A 95% alumina ceramic was chosen because of its good thermal, electrical and high-temperature properties. The thermal conductivity of the 95% alumina ceramic is approximately 12 BTU/hr/ft/°F, which is about that of stainless steel. The high-temperature ceramic is necessary since most of the critical processes for module fabrication are executed at 300° to 800°C.

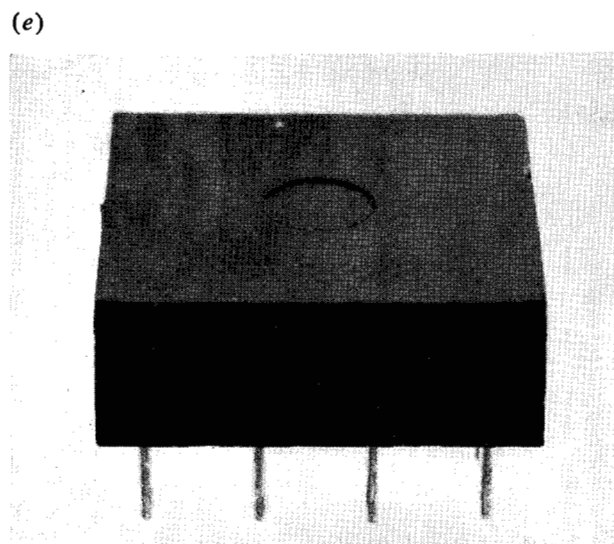
The interconnection land pattern is printed on the substrate, as indicated in Fig. 3a. Inks containing noble



(c)



(d)



(e)

metals with a glass frit binder are used. Stencil screening techniques are used to print the land pattern, which is then fired onto the substrate at about 800°C. During the firing, the glass frit reacts with the alumina substrate to form an intermediate oxide phase. This oxide serves as a binder between the metallic particles and the alumina. The typical as-screened thickness of conductive lines is 0.5 mil.

The resistors are printed by the same methods as the land materials. The resistor material³ is a palladium-silver-glass composition dispersed in an organic vehicle. When the screened resistor paste is fired at about 800°C, palladium oxide forms in a matrix of the palladium-silver-glass binder. The palladium oxide controls the electrical properties of the resistor. In addition, the temperature dependence of carrier concentration yields a temperature coefficient of resistance that is a parabolic function of temperature. Changes in resistor composition and screening conditions can produce a resistivity range of 50 to 50,000 ohms per square. The temperature coefficient in the range 25° to 100°C is somewhat dependent on the resistivity of the paste. For example, it is approximately +350 ppm/°C for the 3,000 ohms/square paste, and +200 ppm/°C for 5,000 ohms/square paste. These resistors can withstand severe conditions of temperature and humidity with no protective overcoat. Life test data are given in the section "Some Test Results".

• Pins

In the next step, copper pins approximately 230 mils long and 20 mils in diameter are inserted into the holes in the substrate. Mechanical forces are applied, causing the metal to flow above and below the substrate. Such a pin will withstand, typically, a pull test of 15 lbs. Figure 3b is a general view of a pinned module. The tool that upsets the pins forms them simultaneously to a spacing of 125 ± 1 mils, thus greatly reducing the required tolerance on the holes in the substrate.

• Solder tinning

The entire module is next immersed in a solder bath at 300°C. Only the lands and pins are wetted by this solder. The solder operation not only insures a good electrical connection between the pins and the lands, but also lowers the series resistance and provides the solder required for joining the land to the semiconductor chip. For example, line widths of 0.005" are reduced in resistance from 20 to 5 ohms/inch, 0.010" width lines from 11 to 1 ohms/inch and 0.015" width lines from 7 to 0.6 ohms/inch after they have been tinned.

Uniform solder height across the module is important. This uniformity is particularly important on the chip attachment pads so that a good solder fillet is obtained

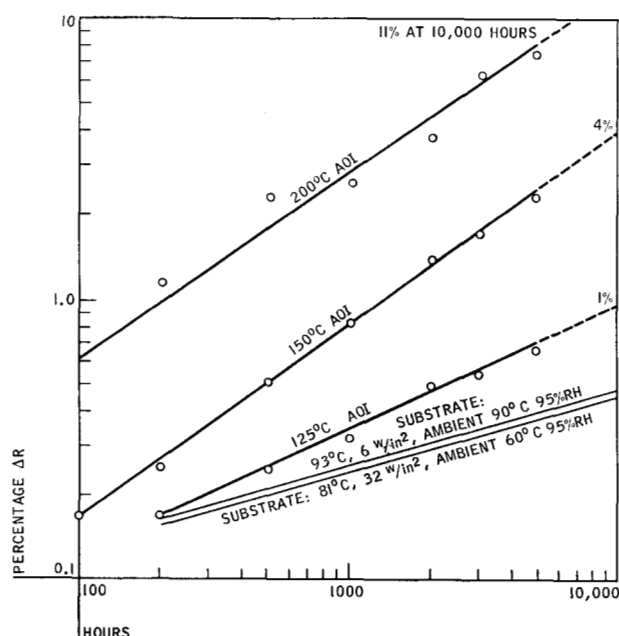


Figure 4 Drift of glaze resistors on fully processed modules.

from the pad to the ball. To assure this even solder height, the topology of the pad is designed with care.

• Resistor trimming

At this point, the ohmic values of the resistors have a typical distribution of $\pm 15\%$. To permit an optimized yield for the desired resistor values, the average of the distributions are set 15% lower than the desired values. The resistors are then tailored to the desired value by abrasive trimming. First the module is inserted into a fixture that has nozzles directed at each resistor. As the module moves under these nozzles, the fine abrasive stream then erodes the resistor, reducing the resistor width and raising the resistance value. Each nozzle is turned off automatically when the desired resistance value is reached. The resistors can readily be trimmed to better than $\pm 1\%$ of the desired value. Resistors are designed to have sufficient area, so that even after the theoretical maximum trimming (30%), they remain within a power density limitation of 15 watts per square inch of active resistor material. A trimmed resistor, showing the area eroded by abrasion, is shown in Fig. 1a.

• Joining chips to substrate

After the passive components on the substrate are tested, the semiconductor chips are joined to the appropriate attachment pads on the substrate. After the pads are fluxed, the chip devices are positioned and gently pushed into the solder layer on the chip attachment pad. The flux and the cold flow of the solder serve to hold the chips in position during subsequent handling until the solder is

Figure 5 Histogram of distribution plots for ΔI_{EBO} relative to I_{EBO} at $t = 0$ for 1,000, 2,000 and 5,000 hrs. $\Delta I_{EBO} = [I_{EBO} - I_{EBO \text{ initial}}]$. I_{EBO} measured at V_{BE} of 3 V at a 75°C temperature ambient.

reflowed. Figure 3c shows a side view of a semiconductor chip positioned on the module solder lands prior to solder reflow. When heat is applied to the module, the solder melts or reflows and wets the balls on the semiconductor chip to create solder fillets at each ball. The side view of a chip after reflow is shown in Fig. 3d. The chip has now been electrically and mechanically joined to the substrate. All chips are joined to the substrate simultaneously.

• Completed modules

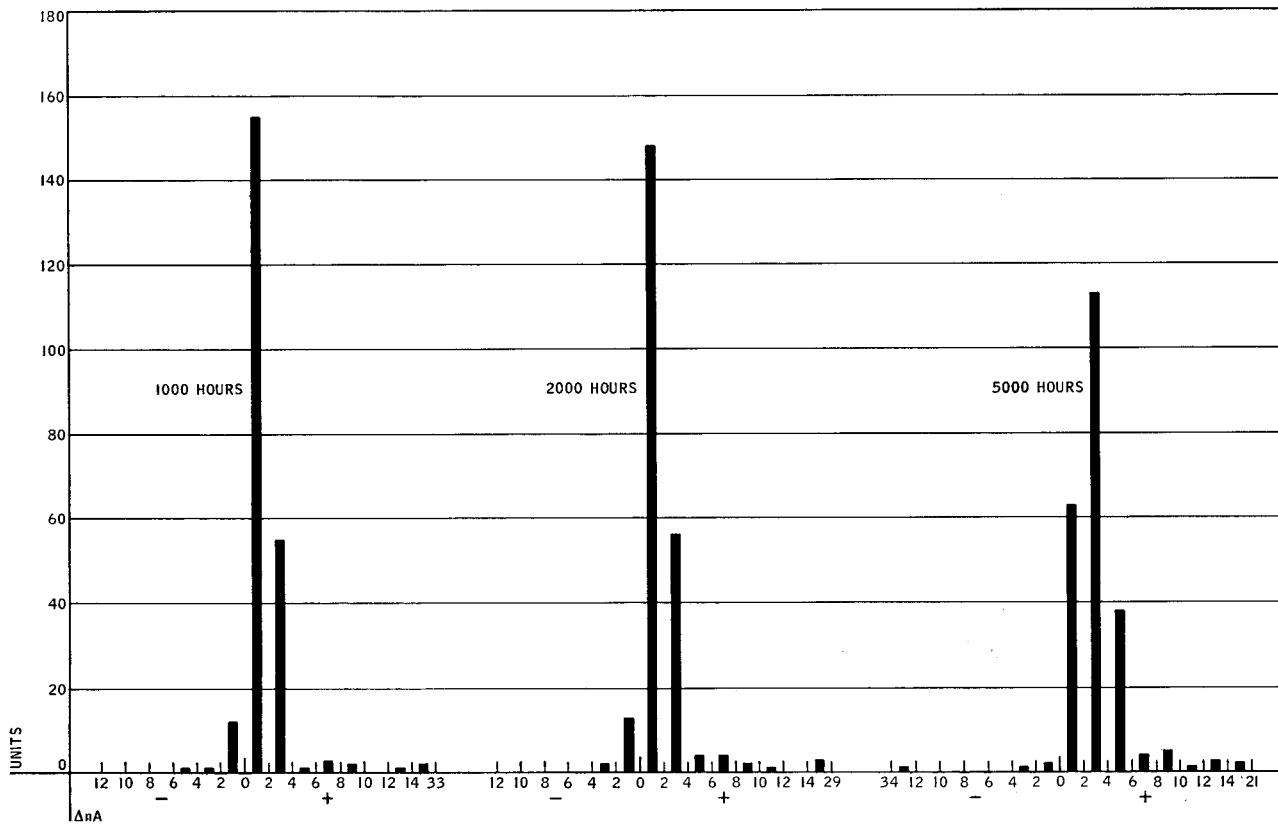
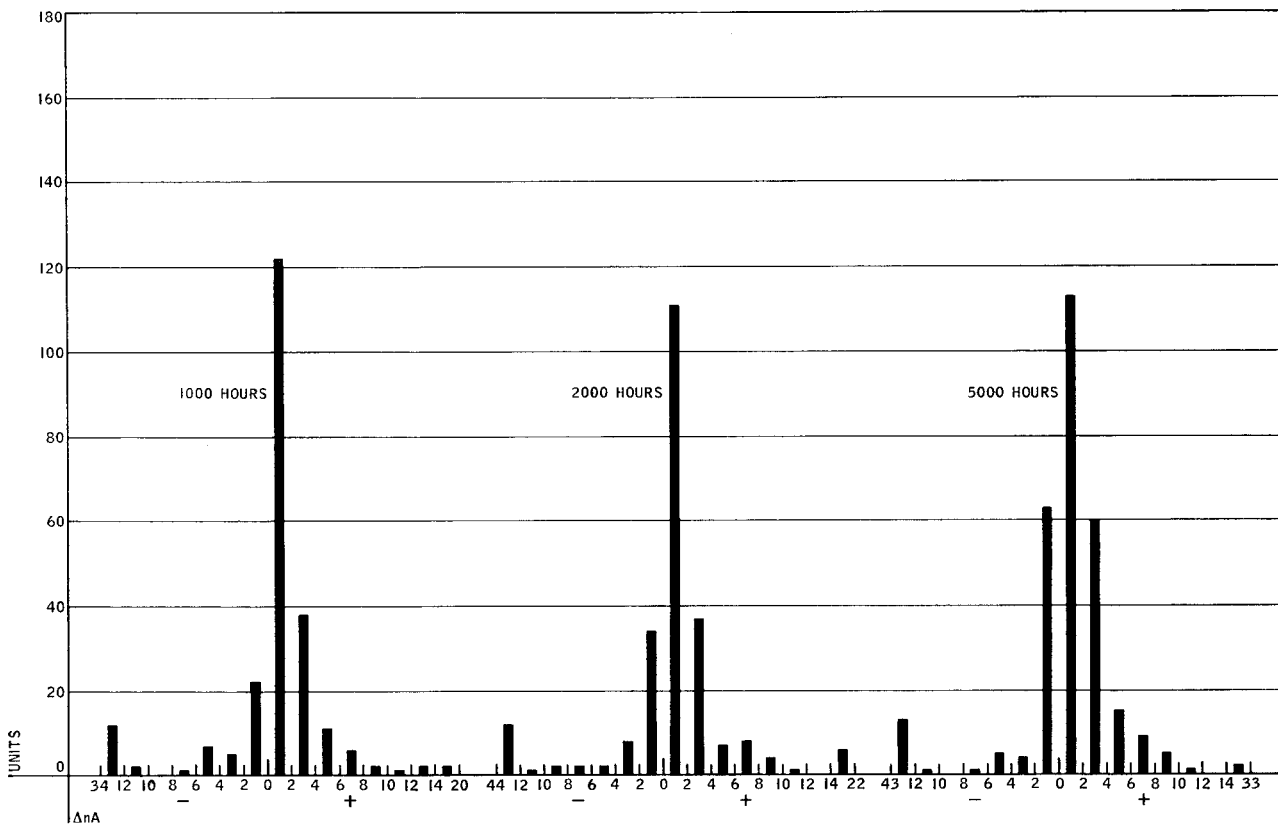
Figure 1a shows an over-all view of a completed module before the protective coating was added. Although none of the components require a hermetically sealed enclosure, the modules are coated with plastic (Fig. 3e) to protect the components mechanically and reduce corrosion of the solder lands under conditions of high humidity.

• Some test results

The resistors and semiconductor devices have been exposed to severe environmental stress conditions for long periods of time to determine stability under non-hermetically sealed conditions. Figure 4 shows 5,000- and 10,000-hour data on resistor drift under various stress conditions. Note that resistance increased with time, although slight negative drifts do occur during the first 200 hours. Drift in these resistors is largely a function of temperature, and the resistors are generally insensitive to humidity or power fluctuations. The data shown are for medium-resistivity materials (500 to 3,000 ohms/square).

Figures 5 and 6 indicate parameter behavior, measured at 75°C , after testing 236 transistors for 5000 hours. One group of these devices (48 transistors) had been maintained in an 85°C ambient and power pulsed (150 mW) so that the junction temperature cycled between 85°C and 150°C . A second group (89 transistors) had been stored at 150°C with $V_{CE} = 8 \text{ V}$ and $V_{BE} = -4 \text{ V}$, and the third group had been stored at 85°C , $85\% \text{ RH}$ with $V_{CE} = 8 \text{ V}$ and $V_{BE} = -4 \text{ V}$. The intent of this test was to examine the stability of the glass-encapsulated semiconductor junc-

Figure 6 Histogram of distribution plots for ΔI_{CBO} relative to I_{CBO} at $t = 0$ for 1,000, 2,000 and 5,000 hrs. $\Delta I_{CBO} = [I_{CBO} - I_{CBO \text{ initial}}]$. I_{CBO} measured at V_{CB} of 6 V at a 75°C temperature ambient.



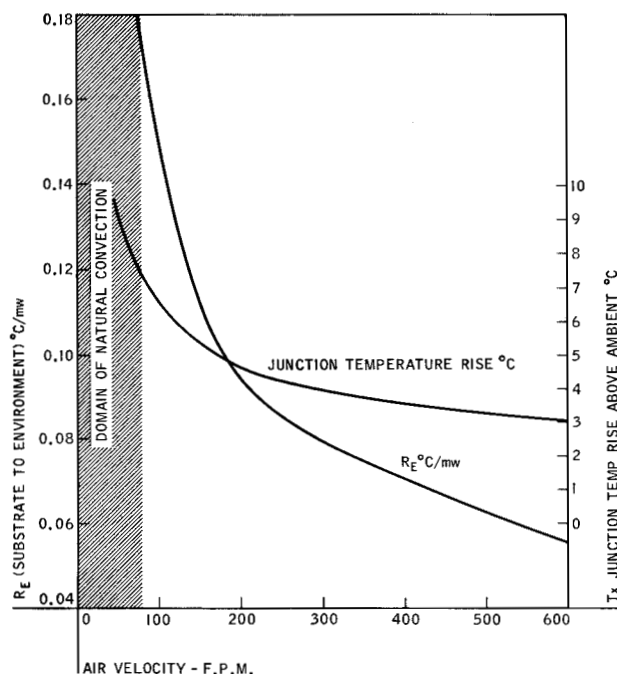


Figure 7 Thermal resistance of substrate and transistor junction temperature rise vs air velocity.

tions. The stability of the data gathered indicates that there are no processes occurring that deteriorate junction properties. Other device parameters, such as junction breakdown voltage, current gain, and the forward characteristics of the junctions, were measured and show similar stability. Three transistors in the 150°C group were removed from this distribution because of gross deviations not related to junction failure mechanisms.

The circuit devices mentioned in this paper have been subjected to integrated gamma radiation doses of 10^8 rads. No significant changes occurred in the passive components. It is also worthy of note that the glassed structure described here significantly reduces the degradation of transistor leakage (and diode reverse currents) in devices subjected to simultaneous reverse bias and ionizing radiation.⁴

• Thermal considerations

As is well known, thermal considerations are of prime importance in microelectronics. Figure 7 shows a plot of the thermal resistance (R_E) of the AOI module and of transistor junction temperature as a function of the air velocity over the module in a typical machine environment. The alumina substrate is essentially an isothermal surface because of its excellent thermal conductivity. The thermal properties of a module then are predicted by the thermal resistance between the chip and the substrate, and the thermal resistance between the substrate and the air. The thermal resistance between the substrate

and a transistor junction is typically $0.13^{\circ}\text{C}/\text{mW}$ and has a worst-case value of $0.15^{\circ}\text{C}/\text{mW}$. The thermal resistance between the substrate and the surrounding air is a function of air velocity. Note that the rise of junction temperature above ambient tends to be small. The circuit designs have been based on a maximum semiconductor junction temperature of 75°C under worst-case environments.

• Extensions of technology

The techniques of fabricating a resistor-transistor-diode module as described above are being utilized to produce circuits for application in the IBM/360 computers. The following sections describe extensions of the technology now under development.

Reactive components

More complex modules incorporating reactive components have been designed. Inductors, capacitors and crossovers can be fabricated on modules by means of graphic arts and solder connection technologies.

• Capacitors

Figure 8a shows capacitors that have been fabricated by alternately screening conductive "plates" and dielectric layers. The capacitors shown have values of 65, 125, 250 and 500 pF. Using specially prepared glass-base compositions having a high dielectric constant, capacitances of $75,000 \text{ pF}/\text{in}^2$ with breakdown voltage greater than 200 volts have been obtained. Abrasion tailoring, similar to that used for the resistor, can be used to obtain capacitance values with better than 5% tolerance.

Single layers of dielectric with metallization on the top and bottom surfaces is a standard form for the chip capacitors. These chips can be incorporated in this type of circuitry when reflow connections are made simultaneously between the bottom metallized surface and a land, and the top metallized surface via a clip to a land. A typical configuration is shown in Fig. 8b.

The dielectrics that are currently available range in K values from 10 to 10,000. The typical chip capacitor has a thickness of 10 mils and a voltage breakdown of 250 V. A capacitor value of $0.01 \mu\text{F}$ can be obtained in a chip having an area of 2200 square mils when a dielectric with a K of 10,000 is used.

In order to obtain high values of capacitance per unit area of substrate, some of the materials available as single chips are processed in the form of laminates. The physical form of a laminate is shown in Fig. 8c. Metallization of the ends permits reflow to substrate lands without the use of metal clip connectors.

• Inductors

Inductors and other magnetic components have been

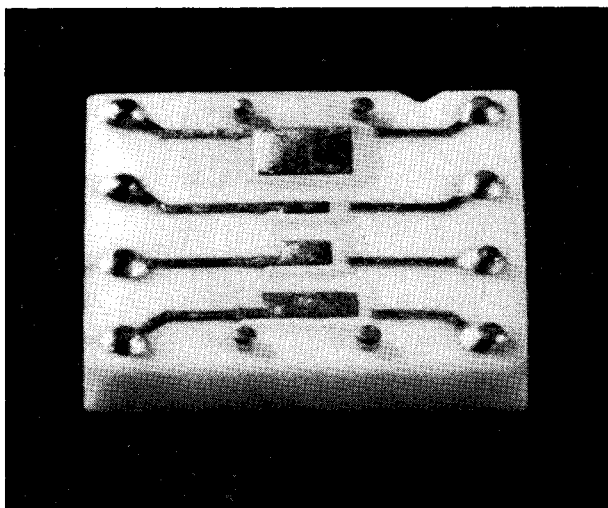
similarly formed by alternate printings of conductors and glass insulation or magnetic material. The simplest inductor pattern is shown in Fig. 9. For five turns of 10-mil conductors spaced 10 mils apart, the typical inductance is 125 nh. The five turns are on top of glass, and the conductor that makes electrical contact to the center of the spiral is under glass. The low frequency inductance of this array becomes 500 nh if ferrite is used instead of glass. This is seen in the center of Fig. 9, and at the right is a toroidal pulse printed transformer. The magnetizing inductance is in the order of 100 nh. For this configuration a printed ferrite is used as the core.

• Crossovers

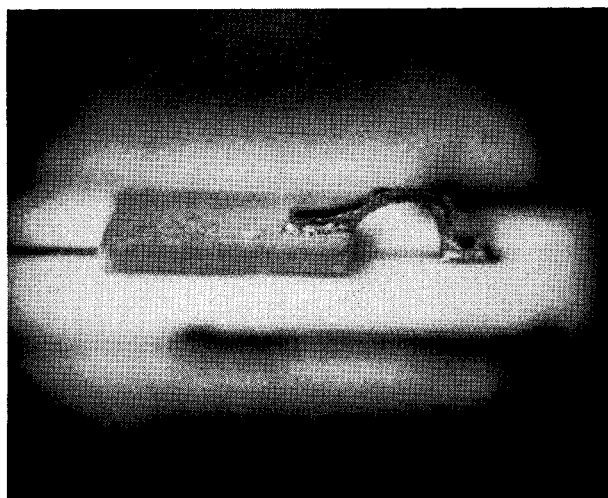
Graphic arts techniques can also be used to fabricate glass crossovers. In fabricating a glass crossover one begins by first printing and firing the lower electrode. Then an area (typically 30×30 mils) of high-temperature glass frit is screened over the electrode. The glass is typically 1.5 to 3 mils thick. After the glass is fired, the second crossing electrode is screened over the glass. For the 30-mil square of glass 2 mils thick, and conductor line widths of 10 mils, the capacitance between electrodes is less than 1 pF and the breakdown voltage greater than 300 V. Figure 10 shows glass crossover test patterns.

Modules with reactive components

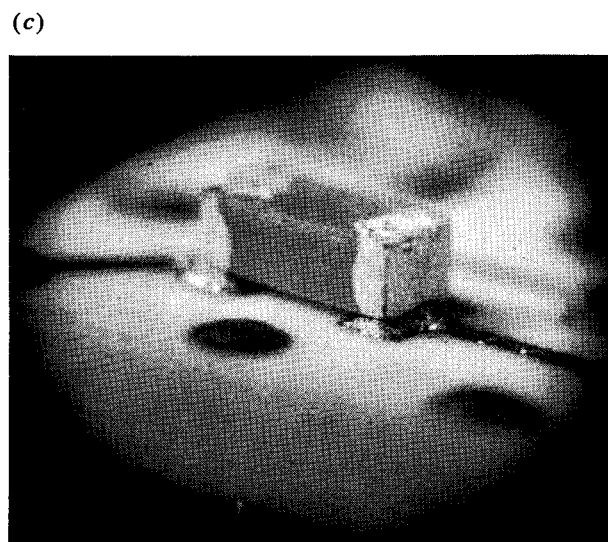
Two modules that combine these technologies are shown in Figs. 11a and 11b. The first module is a 100-Mc frequency-modulated oscillator. Three printed capacitors, three resistors and two transistors populate the top surface of the substrate, and an inductor appears on the bottom surface. The second module is an active coupling stage for very high speed logic. Four discrete, canned tunnel-diode pairs and four resistors appear on the top surface, and a two-layer printed capacitor (conductor-dielectric-conductor-dielectric-conductor) appears on the bottom surface. The capacitance of each unit is about 60,000 pF. The dielectric material is a zinc oxide-bismuth oxide composition with a dielectric constant on the order of 1000. Capacitor values of 500,000 pF/in² are obtained when the material is screened in thicknesses of 0.5 to 0.7 mils. Characterization studies show that the capacitance of this material decreases about 50% in the range 1 kc/sec to 10 Mc/sec and that the shunt resistance decreases from the order of 1000 ohms to the order of 1 to 2 ohms for the same frequency range. The total impedance is about



(a)



(b)



(c)

Figure 8 **Capacitors used in SLT.** (a) Printed capacitor. (b) Single-chip capacitor. (c) Laminated capacitor.

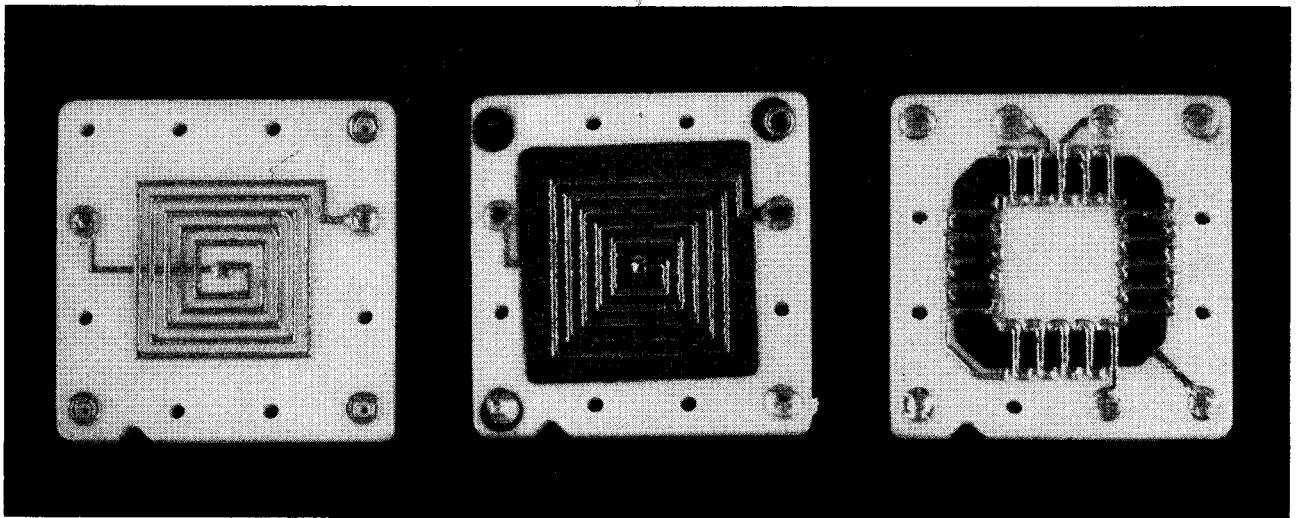
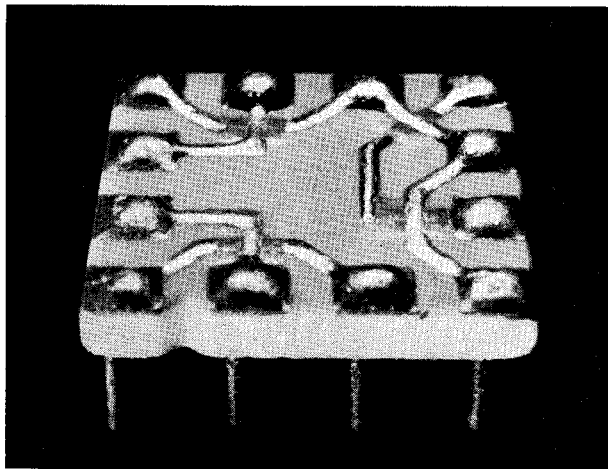


Figure 9 Printed inductors.

Figure 10 Printed crossover.



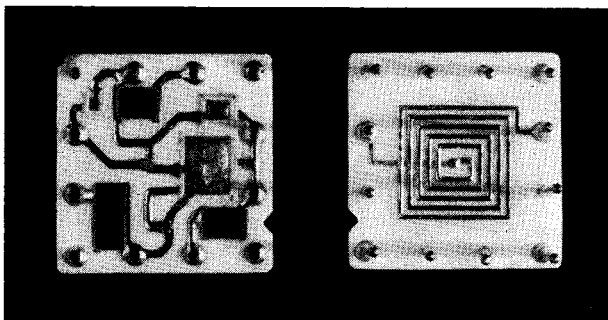
one ohm at 10 Mc/sec giving a damping factor in the order of 95%. These unique attributes provide excellent damping networks, and prevent false switching and power supply ringing in high-speed applications.

Module form factors

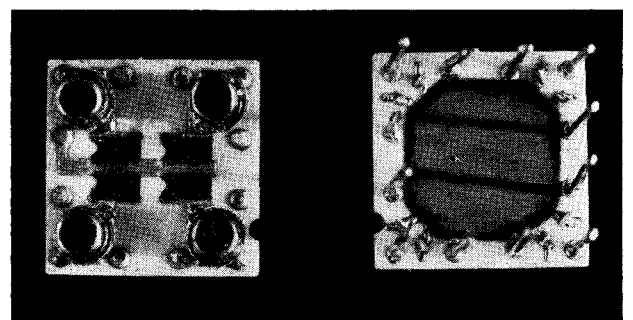
Although a 12-pin substrate is the predominant form factor for modules in the IBM/360 machines, SLT is applicable to a broad range of substrate forms. For higher speed logic requirements, smaller substrates minimize layout problems normally associated with high-frequency circuits and shorter communications delays between modules. For high component density, or for applications requiring complex logic circuits, modules with many circuits can be made on large substrates.

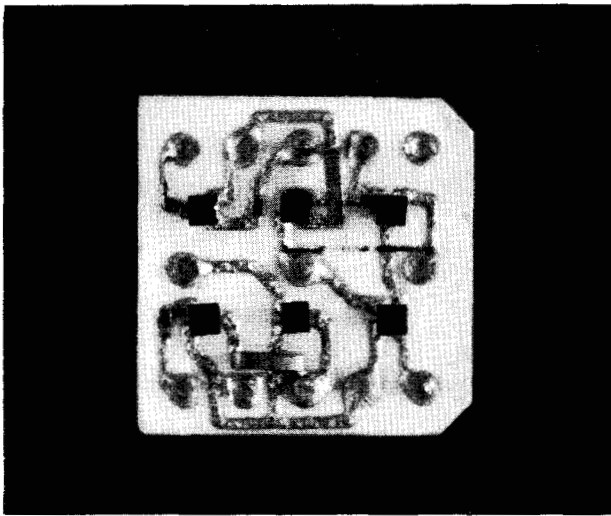
Figure 11 Modules with reactive components. (a) 100-Mc/sec oscillator, top and bottom views. (b) Tunnel diode, with screened capacitor active coupling stage, top and bottom views.

(a)

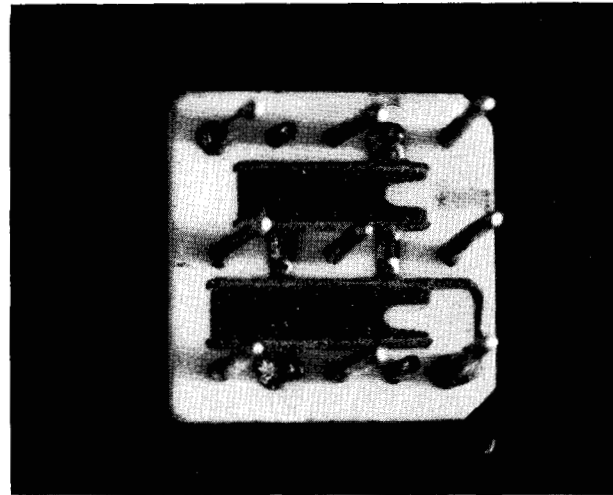


(b)





(a)



(b)

Figure 12 High-speed logic module on small substrate. (a) Top. (b) Bottom.

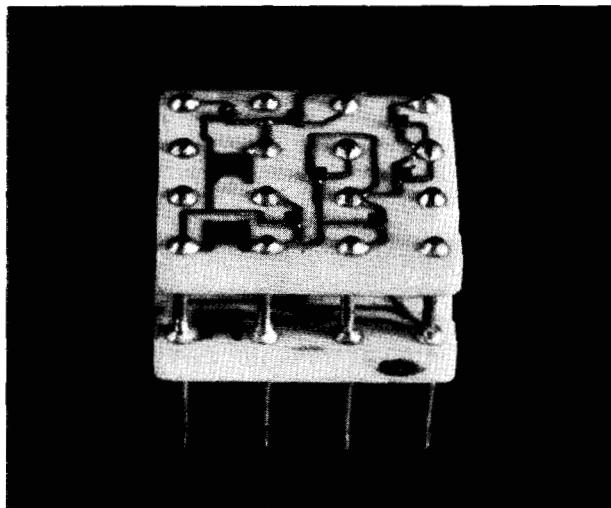


Figure 13 Stacked module.

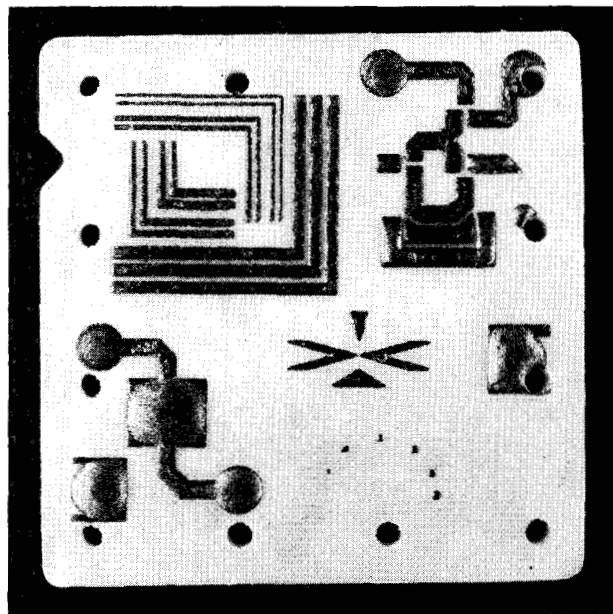


Figure 14 High-definition test pattern.

- High packing density of components

An example of a small module providing high component density and high-speed performance is shown in Fig. 12. The substrate is $0.270'' \times 0.270'' \times 0.040''$, contains 13 pins, and an average of 6 transistors on the top surface and 2 resistors on the bottom surface. Four of

the pins serve as interconnections between the substrate surfaces. Note that this module has two crossovers produced by small metal bridges or staples. The staples are reflowed to the module during the same thermal cycle that joins the chip transistors. Modules of this kind have a performance characteristic of about one nanosecond nominal delay per logic decision.

One method of increasing component packing density is to use stacked substrates. For such a module, individual substrates are processed in the normal manner. Finally, one module is placed on top of the other, and a reflow connection made to each aligned pin. A stacked module is shown in Fig. 13. A total of 11 transistors and 8 resistors comprise the component complement of this particular module.

A second method of increasing component packaging density is to reduce the size of the interconnections and passive components. Figure 14 shows a high-definition test pattern. The smallest lines are 2 mils wide on 7-mil centers. The conductive pastes contained silver and vehicular additives. As a result, this 2-mil line showed no appreciable increase in resistivity over the previously described 15-mil lines. A module fabricated with small, high-power-dissipation resistors is shown in Fig. 15. This module has a total of 12 reduced-size resistors, 8 semiconductor chips and 3 glass crossovers. The module functionally performs 4 AND-INVERT logic statements.

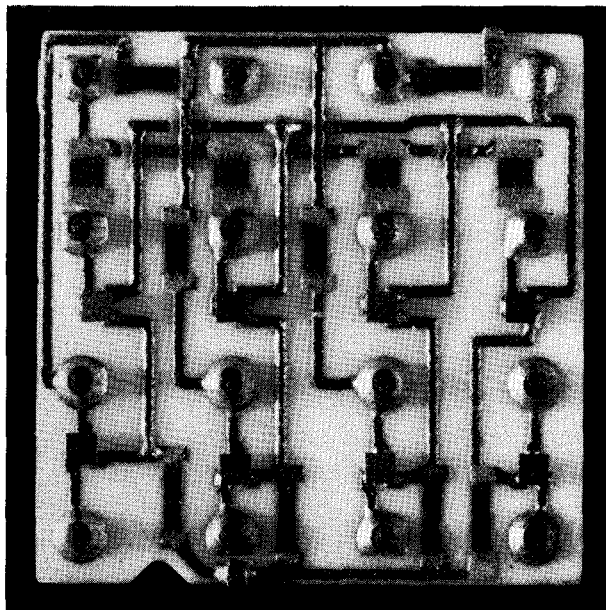
The use of large substrates offers desirable advantages in accommodating the requirements of complex, and/or large logic statement circuits. One of such large developmental modules is shown in Fig. 16. This substrate is $1\frac{7}{8}'' \times 2\frac{1}{2}''$ and contains twenty 5-input OR circuits and four AND circuits, giving a total of 64 resistors and

108 chips (if all circuits are active and fully populated). Not all of the circuits in the illustration are populated with semiconductor chips. The particular logic connectives on this substrate required only 18 transistors and 61 dual diodes. Four screening operations are required: a "character" layer of interconnection circuitry, glass crossovers, resistors, and an over-glass set of crossover connectors. Only the "character" layer need be changed to accommodate other logic statements. A total of 50 crossover areas exist, 21 of which are 180×340 mils.

• *Module mounting of high-power devices*

Modules may also be used in high-power dissipation circuits such as those often used in memories. Solderable glass-encapsulated driver devices can be reflowed directly to land patterns on the substrate, as shown in Fig. 17. Individual clips can be reflowed to form connections to the emitter and base on the top surface of the chip. The reflow of the chip on its back side not only serves as the electrical contact for the collector, it also provides the large contact area helpful in reducing the thermal resistance between the chip and the substrate. The thermal resistance between transistor and substrate for this chip joining process is typically $0.04^\circ\text{C}/\text{mW}$. Performance at one-watt levels is thus obtainable with alumina substrates. Two-watt performance has been obtained with the use of beryllia ceramic substrates, and/or heat sink configurations to lower the effective thermal resistance of the package.

Figure 15 Four-AI module using small, high-power-dissipation resistors.



Conclusions

The approaches taken in developing SLT were directed toward solving some of the problems generally prevalent in other forms of microelectronics packages. The technology that resulted from the development efforts has shown that hybrid, integrated circuits can be fabricated for high performance and flexibility of application. The processes that are employed in the fabrication of both active and passive components are a major factor in the quality and reliability. This technology has a broad scope of packaging dimensions that may be matched to the applications requirements—small substrates for high-speed performance (nanosecond switching) and high component density, or large substrates for complex subsystems.

The advantages of this technology can be listed as follows:

1. Graphic arts techniques are used to produce high-quality passive components having tight tolerances—resistors, inductors, and capacitors on a ceramic substrate.
2. Silicon planar glass-encapsulated transistors and diodes are used. These glassed devices do not require a hermetically sealed enclosure to provide long life and highly

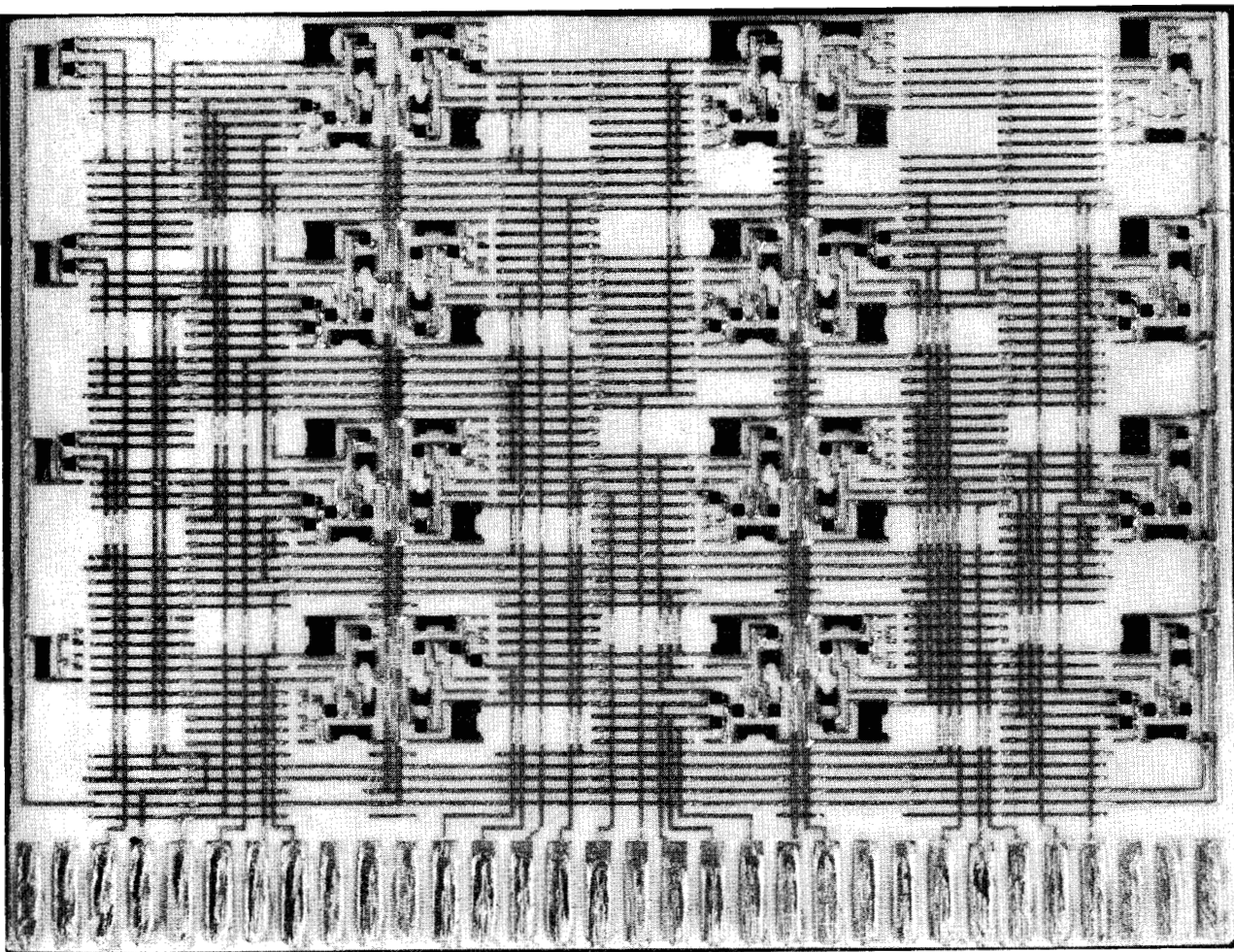


Figure 16 Large substrate (see text).

reliable performance. A soldering process is used to join these "chip" devices electrically and mechanically into the passive components circuit.

3. The ability to obtain optimized parameter control for the transistors and diodes while simultaneously but independently exercising a tight tolerance control on a wide range of resistors or other passive components permits the attainment of close to maximum circuit performance.

4. A hermetic package is not mandatory.

5. Thermal difficulties are minimized through the use of materials and configurations that have low thermal resistance. In addition, the tight-tolerance circuit components reduce the power required to perform a given circuit function.

6. Parasitic interactions are reduced to a minimum.

Figure 17 Mounting technique for power device.



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